M5M4S16S30CTP-07, -08, -10

16M (2097152 - word by 8-bit) Synchrounous DRAM

Preliminary
Some of the contents are subject to change without notice.

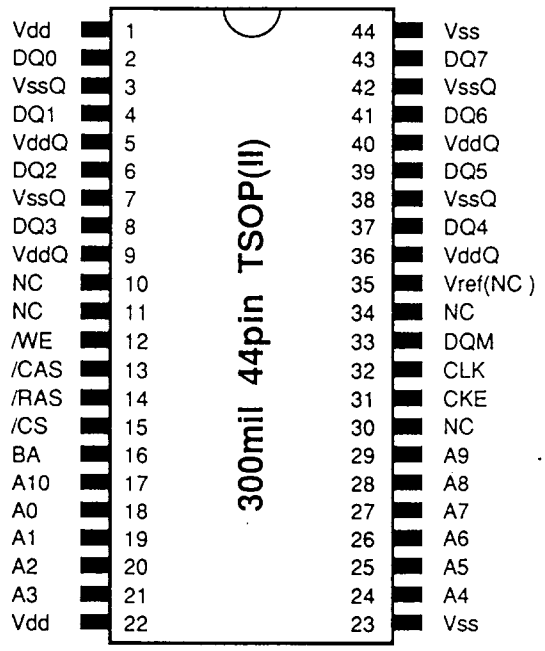
DESCRIPTION

The M5M4S16S30CTP is a 2-bank x 1048576-word x 8-bit Synchronous DRAM.

FEATURES

- Single 3.3±0.3v power supply
- Clock frequency 150MHz / 125MHz / 100MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA (Bank Address)
- /CAS latency- 1 / 2 / 3 / 4 (programmable)
- Burst length- 1 / 2 / 4 / 8 (programmable)
- Burst type- sequential / interleave (programmable)
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycles /64ms
- SSTL Interface (-10; LVTTL & SSTL)
- 300-mil, 44-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

PIN CONFIGURATION (TOP VIEW)



	Max. Frequency	CLK Access Time @CL=4
M5M4S16S30CTP-07	150MHz	5ns
M5M4S16S30CTP-08	125MHz	6ns
M5M4S16S30CTP-10	100MHz	8ns
M5M4V16S30CTP-10 (LVTTL)	100MHz	8ns

CLK	: Master Clock
CKE	: Clock Enable
/CS	: Chip Select
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQ0-7	: Data I/O
DQM	: Output Disable/ Write Mask
A0-10	: Address Input
BA	: Bank Address
Vdd	: Power Supply
VddQ	: Power Supply for Output
Vss	: Ground
VssQ	: Ground for Output

Mode Register

Mode Register Set (Programming mode)

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	LTMODE			BT	BL		

Latency Mode (LT Field)

Bits (654)	CAS Latency
001	1
010	2
011	3
100	4

Burst Type (BT Field)

Bit 3	Type
0	Sequential
1	Interleave

Burst Length (BL Field)

Bits (210)	Burst Length
000	1
001	2
010	4
011	8

Burst Address Ordering for Burst Length (BL = 4)

Start Address (Column Address Bits A1, A0)	Burst Type = Interleave	Burst Type = Sequential
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 0, 3, 2	1, 2, 3, 0
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 2, 1, 0	3, 0, 1, 2

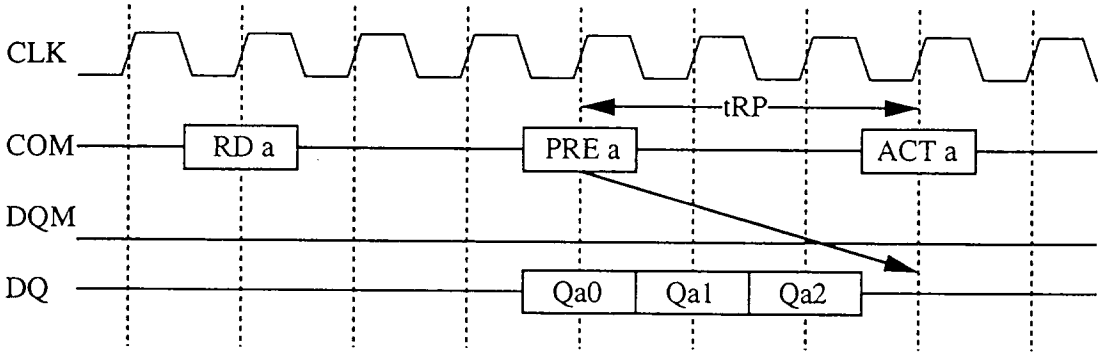
Command Truth Table

COMMAND	CKE		/CS	/RAS	/CAS	/WE	BA	A10	A9-A0
	n-1	n							
Row Address Strobe & Bank Activate	H	X	L	L	H	H	V	V	V
Column Address Strobe & Read	H	X	L	H	L	H	V	L	V
Column AddressStrobe & Read (with Auto Precharge)	H	X	L	H	L	H	V	H	V
Column Address Strobe & Write	H	X	L	H	L	L	V	L	V
Column Address Strobe & Write (with Auto Precharge)	H	X	L	H	L	L	V	H	V
Precharge (single bank)	H	X	L	L	H	L	V	L	X
Precharge (all banks)	H	X	L	L	H	L	X	H	X
Auto Refresh	H	H	L	L	L	H	X	X	X
Mode Register Set	H	H	L	L	L	L	L	L	V
Power Down Entry 1	H	L	H	X	X	X	X	X	X
Power Down Entry 2	H	L	L	H	H	H	X	X	X
Self-Refresh Entry	H	L	L	L	L	H	X	X	X
Exit (Self-Refresh / Power Down)	L	H	H	X	X	X	X	X	X
Exit (Self-Refresh / Power Down)	L	H	L	H	H	H	X	X	X
Deselect Device	H	X	H	X	X	X	X	X	X
Deselect Device	H	X	L	H	H	H	X	X	X
Clock Suspend	L	L	X	X	X	X	X	X	X
Reserved for Future Use	H	X	L	H	H	L	X	X	X

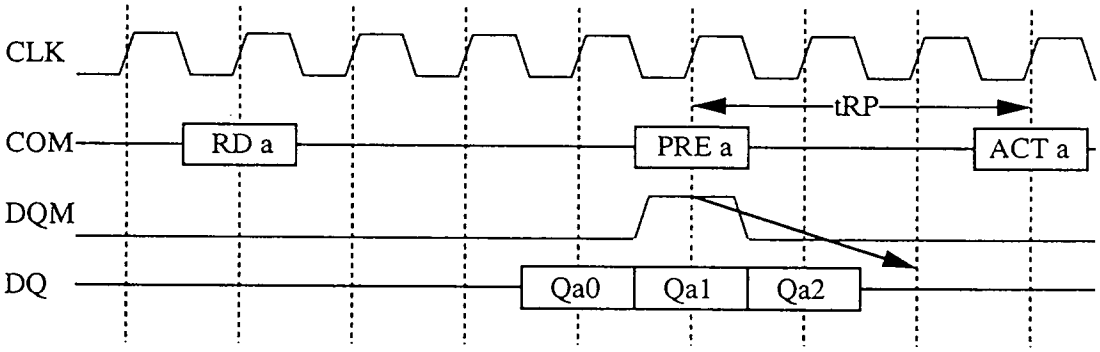
Functional Description

Precharge Termination of Burst Read

Burst Read is terminated by Precharge of the same bank.



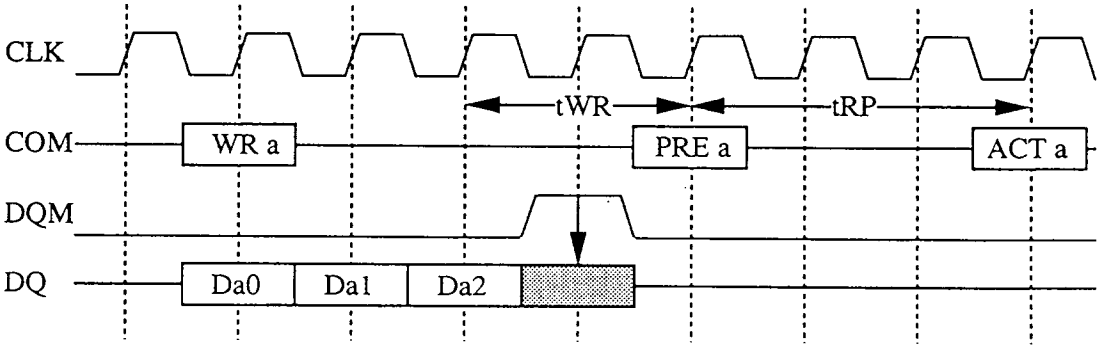
DQ becomes Hi-Z automatically. In this case Latency (Pre to HiZ) is 3.



DQ becomes Hi-Z by DQM. In this case Latency (DQM to HiZ) is 2 (JEDEC std).

Precharge Termination of Burst Write

Burst Write is terminated by Precharge of the same bank.



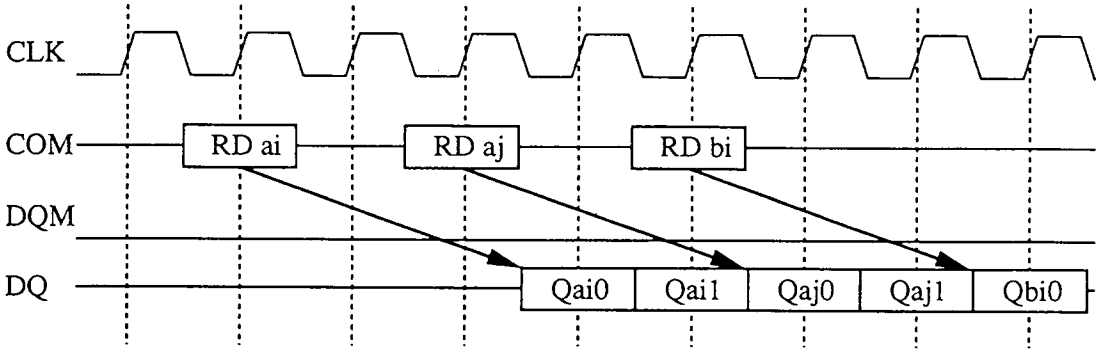
Minimum 2 CLK is necessary from last Din to Precharge (tWR).

Unnecessary Din must be masked by DQM.

In this case Latency (DQM to Din) is 0 (JEDEC std).

Read Interrupted by Read

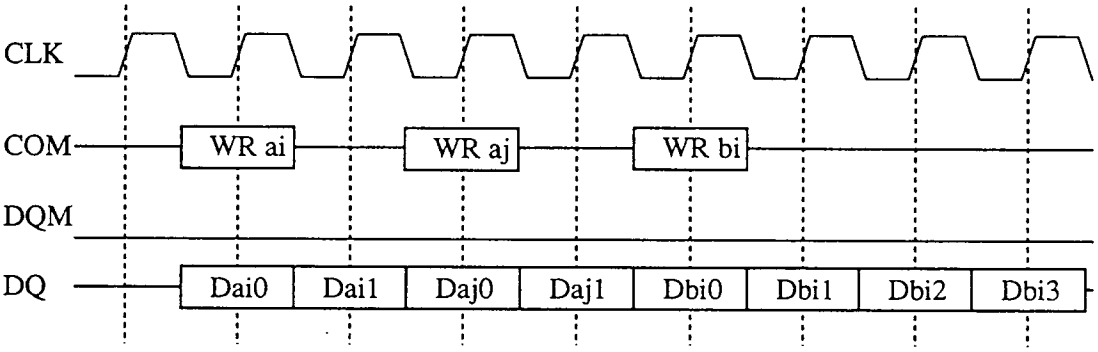
Burst Read is terminated by new Read (either the same or the other bank).



Read to Read delay is minimum 2 CLK (2n rule).

Write Interrupted by Write

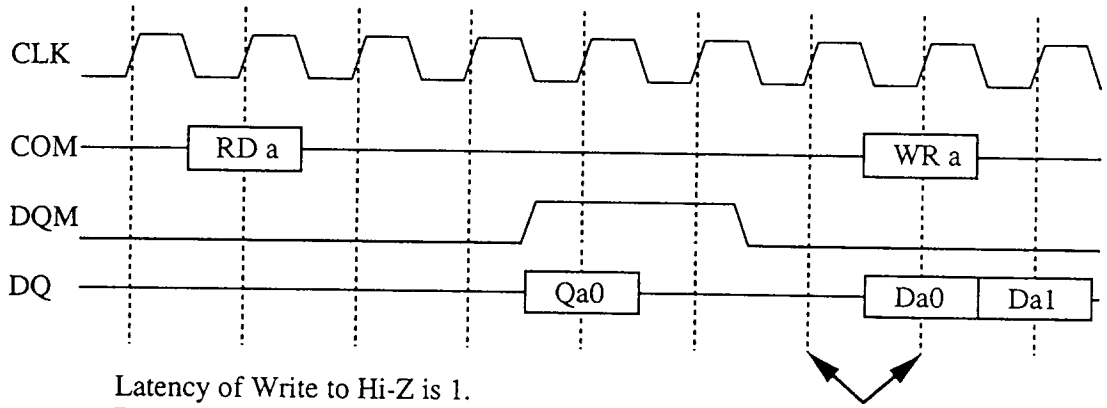
Burst Write is terminated by new Write (either the same or the other bank).



Write to Write delay is minimum 2 CLK (2n rule).

Read Interrupted by Write

Burst Read is terminated by new Write (either the same or the other bank).

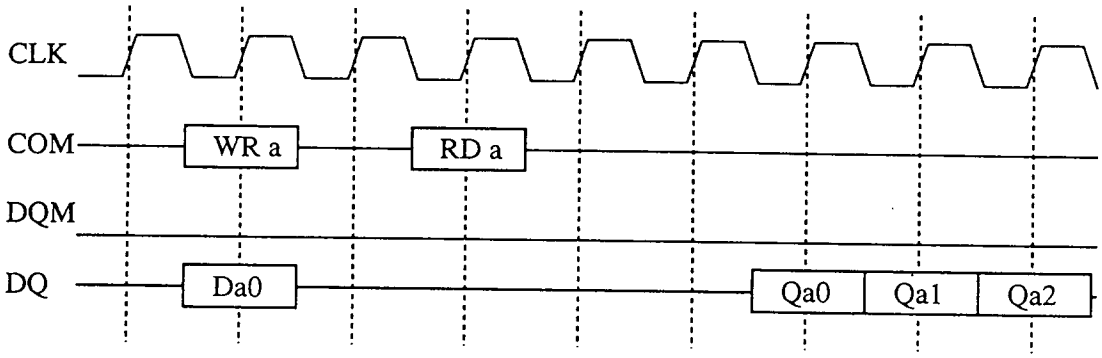


Latency of Write to Hi-Z is 1.
Read to Write delay is minimum 6CLK (2n rule).

Dout should be disabled by DQM.

Write Interrupted by Read

Burst Write is terminated by new Read (either the same or the other bank).



Write to Read delay is minimum 2 CLK (2n rule).

DC Parameters

DC Parameters	Symbol	Min	Max	Unit	Notes
Voltage					
Supply Voltage	Vcc	3	3.6	V	
Input Voltage	Vih	2	4.5	V	
Input Voltage	Vil	-0.6	0.8	V	
Amb. Temp		0	70	℃	
Capacitance					(Ta=25℃, f=1MHz)
Inputs(all)	CI		4	pf	
DQ	Clo		7	pf	

Vref=0.45VddQ

AC Parameters

Parameter	Symbol	Speed Grade		Speed Grade		Speed Grade		Speed Grade		Unit	Notes
					100		125		150	MHz	
		Min	Max	Min	Max	Min	Max	Min	Max	ns	
Clock Period	Tclk			10		8		6.7			CAS Latency=4
Clock High Time	Tch			4		3		2.5			Rated @Vref
Clock Low Time	Tcl			4		3		2.5			
Input Setup Time	Tsi			2		1.5		1.5			
Input Hold Time	Thi			1		1		0.5			
Output Valid From Clock	Tac				8		6		5		Rated @Vref
Output Hold From Clock	Toh			3		2.5		2			
CAS to CAS Delay	Tccd			2						Tclk	
CAS Bank Delay	Tcbd			1						Tclk	
CKÈ to Clock Disable	Tcke			1						Tclk	
DQM to input Data Delay	Tdqd			0						Tclk	
Write Cmd. to input Data Delay	Tdwd			0						Tclk	
DQM to Data out HiZ for read	Tdqz			2						Tclk	
DQM to Data mask for write	Tdqm			0						Tclk	Data Masked on the same clock
RAS Cycle Time	Trc			100		90		80		ns	
RAS Precharge Time	Trp			30		30		26		ns	
RAS Active Time	Tras			60	10000	55	10000	50	10000	ns	
RAS to RAS Bank Active Delay	Trrd			20		16		13		ns	
RAS to CAS Delay	Trcd			30		24		20		ns	
Write Recovery	Twr			20		16		13		ns	

* Symbol names may be changed in Full Feature Version.